SY89853U

Precision Low-Power Dual 2:1 LVPECL MUX with Internal Termination

General Description

The SY89853U features two, low jitter 2:1 differential multiplexers with 100K LVPECL (800mV) compatible outputs, capable of handling clocks up to 2.5GHz and data streams up to 2.5Gbps.

The SY89853U differential inputs include Micrel's unique, 3-input termination architecture that allows users to interface to any differential signal (AC- or DC-Coupled) as small as 100mV without any level shifting or termination resistors networks in the signal path. The result is a clean, stub-free, low jitter interface solution. The differential 800mV LVPECL outputs have fast rise/fall times guaranteed to be less than 180ps.

The SY89853U operates from a 2.5V ±5% or a 3.3V ±10% supply, and is guaranteed over the full industrial temperature range (–40°C to +85°C). For applications that require higher performance, consider the SY58026U. The SY89853U is part of Micrel's Precision Edge® product family.

All support documentation can be found on Micrel's web site at www.micrel.com.

Precision Edge®

Features

- Dual 2:1 MUX, each channel selects from inputs
- Unique, patent-pending input isolation design minimizes crosstalk
- Low power 210mW (V_{CC} = 2.5V)
- Guaranteed AC performance over temperature and voltage:
  - DC-to->2.5Gbps data rate throughput
  - <360ps IN-to-Q t_{pd}
  - <180ps t_r/t_f times
- Ultra-low jitter design:
  - <1ps$_{RMS}$ random jitter
  - <10ps$_{PP}$ deterministic jitter
  - <10ps$_{PP}$ total jitter (clock)
  - <0.7ps$_{RMS}$ crosstalk-induced jitter
- Unique, patent-pending 50Ω input termination and VT pin accepts DC- and AC-coupled inputs (CML, LVDS, PECL)
- 800mV LVPECL output swing
- Power supply 2.5V ±5% or 3.3V ±10%
- –40°C to +85°C temperature range
- Available in 32-pin (5mm x 5mm) MLF® package

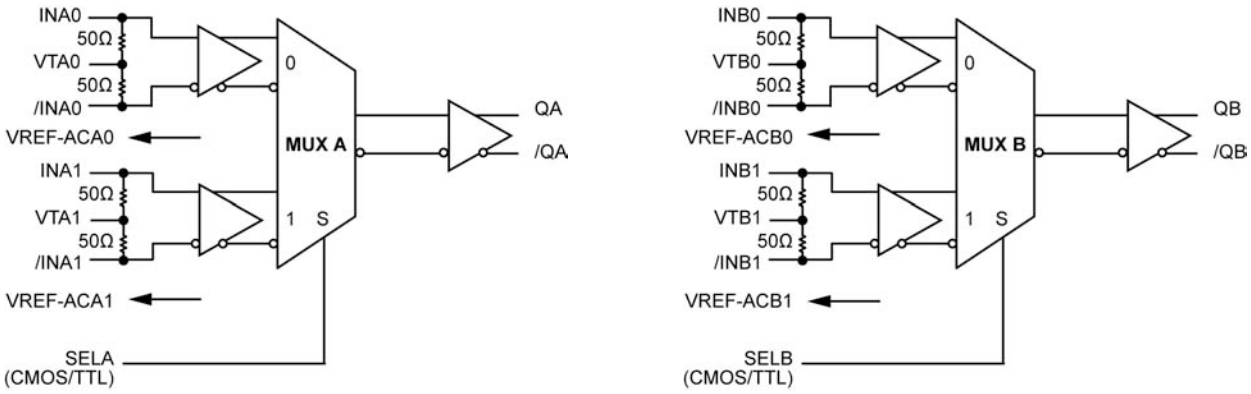
Applications

- Data communication systems
- All SONET OC-3 to OC-48 applications
- All Fibre Channel applications
- All GigE applications

Markets

- LAN/WAN communication
- Enterprise servers
- ATE
- Test and measurement

Functional Block Diagram



Truth Table

SEL	Q
0	IN0 Input Select
1	IN1 Input Select

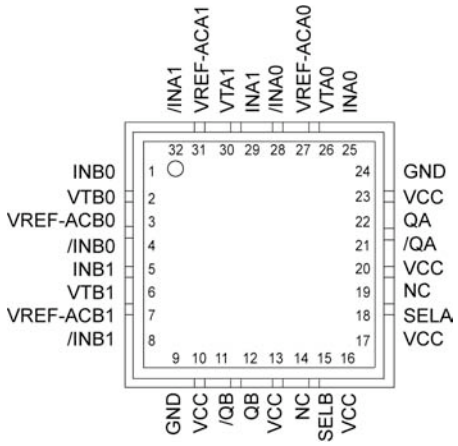
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89853UMG	MLF-32	Industrial	SY89853U with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY89853UMGTR[2]	MLF-32	Industrial	SY89853U with Pb-Free bar-line indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25ºC, DC Electricals only.
2. Tape and Reel.

Pin Configuration



32-Pin MLF® (MLF-32)

Pin Description

Pin Number	Pin Name	Pin Function
25, 28, 29, 32 1, 4 5, 8	INA0, /INA0, INA1, /INA1, INB0, /INB0, INB1, /INB1	Differential Inputs: These input pairs are the differential signal inputs to the device. Inputs accept AC- or DC-coupled signals as small as 100mV. Each pin of a pair internally terminates to a VT pin through 50Ω. Note that these inputs will default to an indeterminate state if left open. Connecting one input to VCC and the complementary input-to-GND through 1kΩ resistor can terminate unused differential input pairs. The VT pin is to be left open in this configuration. Please refer to the "Input Interface Applications" section for more details.
10, 13, 16, 17, 20, 23	VCC	Positive power supply. Bypass with 0.1µF//0.01µF low ESR capacitors. The 0.01µF capacitor should be as close to VCC pin as possible.
14, 19	NC	Not connected.
18 15	SELA, SELB	Bank A and Bank B Input Channel Select (TTL/CMOS): These TTL/CMOS-compatible inputs select the inputs to the multiplexers. These inputs are internally connected to a 25kΩ pull-up resistor and will default to logic HIGH state if left open.
22, 21 12, 11	QA, /QA, QB, /QB	Differential Outputs: These LVPECL output pairs are the outputs of the device. They are a logic function of the INA0, INA1, INB0, INB1 and SELA and SELB inputs. Please refer to the "Truth Table" below for details.
26, 30 2, 6	VTA0, VTA1 VTB0, VTB1	Input Termination Center-Tap: Each side of the differential input pair terminates to a VT pin. The VTA0, VTA1, VTB0, VTB1 pins provide a center-tap to a termination network for maximum interface flexibility. See "Input Interface Applications" section for details.
27 31 3 7	VREF-ACA0, VREF-ACA1, VREF-ACB0, VREF-ACB1	Reference Voltages: These reference voltage outputs are equivalent to V_{CC}-1.2V. They are used for AC-coupled inputs. Connect VREF-AC directly to the VT pin and bypass with 0.01µF low ESR capacitor to V_{CC}. See "Input Interface Applications" section. Maximum sink/source current is ±1.5mA.
9, 24	GND, Exposed Pad	Ground: Ground pins and exposed pad must be connected to the same ground plane.

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}
LVPECL Output Current (I_{OUT})
  Continuous ..... ±50mA
  Surge ..... ±100mA
Termination Current
  Source or Sink Current on V_T ..... ±50mA
Input Current
  Source or Sink Current on IN, /IN ..... ±50mA
Current (V_{REF-AC})
  Source or Sink Current on V_{REF-AC} ..... ±2mA
Lead Temperature (soldering, 20sec.) ..... 260°C
Storage Temperature (T_s) ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{CC}) ..... +2.375V to +2.625V
  ..... +3.0V to +3.6V
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance[3]
  MLF® (θ_{JA})
    Still-Air ..... 35°C/W
    500lfpm ..... 28°C/W
  MLF® (ψ_{JB})
    Junction-to-Board ..... 16°C/W

DC Electrical Characteristics[4]

T_A = –40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply	V_{CC} = 2.5V V_{CC} = 3.3V	2.375 3.0	2.5 3.3	2.625 3.6	V V
I_{CC}	Power Supply Current	No load, max. V_{CC}.		65	85	mA
R_{IN}	Input Resistance (IN-to-VT)		45	50	55	Ω
R_{DIFF_IN}	Differential Input Resistance (IN-to-/IN)		90	100	110	Ω
V_{IH}	Input High Voltage (IN, /IN)	Note 5	V_{CC}– 1.6		V_{CC}	V
V_{IL}	Input Low Voltage (IN, /IN)		0		V_{IH}– 0.1	V
V_{IN}	Input Voltage Swing (IN-to-/IN)	See Figure 1a.	0.1		1.7	V
V_{DIFF_IN}	Differential Input Voltage Swing |IN - /IN|	See Figure 1b.	0.2			V
V_{T_IN}	Maximum Input Voltage (IN-to-V_T)				1.28	V
V_{REF-AC}	Output Reference Voltage		V_{CC}– 1.3	V_{CC}– 1.2	V_{CC}– 1.1	V

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB. θ_{JA} and ψ_{JB} values are determined for a 4-layer board in still-air, unless otherwise stated.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
5. V_{IH} (min) not lower than 1.2V.

LVPECL Outputs DC Electrical Characteristics[5]

V_{CC} = 2.5V ±5% or 3.3V ±10%; R_L = 50Ω to V_{CC}–2V; T_A = –40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output High Voltage (Q, /Q)		V_{CC}–1.145		V_{CC}–0.895	V
V_{OL}	Output Low Voltage (Q, /Q)		V_{CC}–1.945		V_{CC}–1.695	V
V_{OUT}	Output Voltage Swing (Q, /Q)	See Figure 1a.	400	800		mV
$V_{DIFF-OUT}$	Differential Output Voltage Swing (Q, /Q)	See Figure 1b.	800	1600		mV

LVTTL/CMOS DC Electrical Characteristics[5]

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A = –40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
I_{IH}	Input High Current	V_{IN} = V_{CC}			75	µA
I_{IL}	Input Low Current	V_{IN} = 0.5V	–300			µA

Notes:

5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC Electrical Characteristics[6]

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A = –40°C to + 85°C, R_L = 50Ω to V_{CC}–2V, unless otherwise stated.

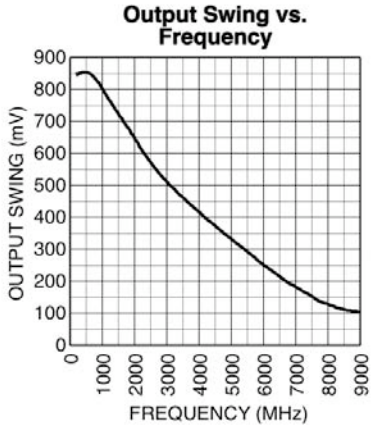
Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Operating Frequency	NRZ Data	2.5			Gbps
		Clock, V_{OUT} > 400mV	2.5			GHz
t_{pd}	Propagation Delay					
	IN-to-Q		160	250	360	ps
	SEL-to-Q		100	260	400	ps
t_{pd} Tempco	Differential Propagation Delay Temperature Coefficient			143		fs/ ºC
t_{SKEW}	Input-to-Input Skew (Within-bank)	Note 7		10	20	ps
	Bank-to-Bank Skew	Note 8		12	25	ps
t_{JITTER}	Data					
	Random Jitter (RJ)	Note 9			1	ps_{RMS}
	Deterministic Jitter (DJ)	Note 10			10	ps_{PP}
	Clock					
	Cycle-to-Cycle Jitter	Note 11			1	ps_{RMS}
	Total Jitter (TJ)	Note 12			10	ps_{PP}
	Crosstalk-Induced Jitter					
	Channel-to-Channel (Within-bank)	Note 13, within-bank			0.7	ps_{RMS}
t_r, t_f	Output Rise/Fall Time (20% to 80%)	At full output swing.	50	100	180	ps

Notes:

6. High-speed AC parameters are guaranteed by design and characterization. V_{IN} swing ≥ 100mV, unless otherwise stated.
7. Input-to-input skew is the difference in time between two inputs to the output within a bank.
8. Bank-to-bank skew is the difference in time from input to the output between banks.
9. Random jitter is measured with a K28.7 character pattern, measured at <f_{MAX}.
10. Deterministic jitter is measured at 2.5Gbps with both K28.5 and 2^{23}-1 PRBS pattern.
11. Cycle-to-cycle jitter definition: the variation of periods between adjacent cycles, $T_n - T_{n-1}$ where T is the time between rising edges of the output signal.
12. Total jitter definition: with an ideal clock input of frequency <f_{MAX}, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.
13. Crosstalk is measured at the output while applying two similar differential clock frequencies that are asynchronous with respect to each other at the inputs.

Typical Operating Characteristics

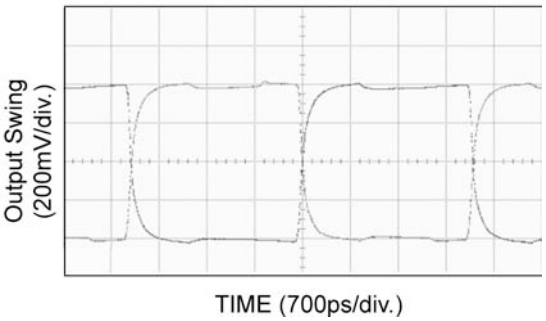
V_{CC} = 3.3V ±10%; T_A = –40°C to + 85°C, R_L = 50Ω to V_{CC}–2V, unless otherwise stated.



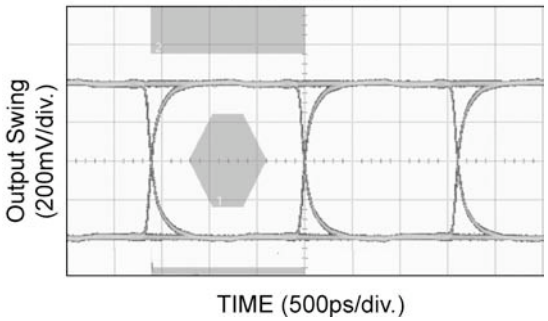
Functional Characteristics

V_{CC} = 3.3V ±10%; T_A = –40°C to + 85°C, R_L = 50Ω to V_{CC}–2V, unless otherwise stated.

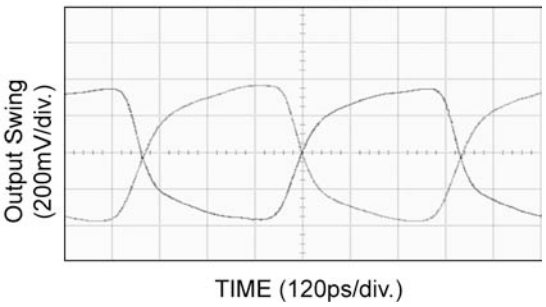
200MHz Output



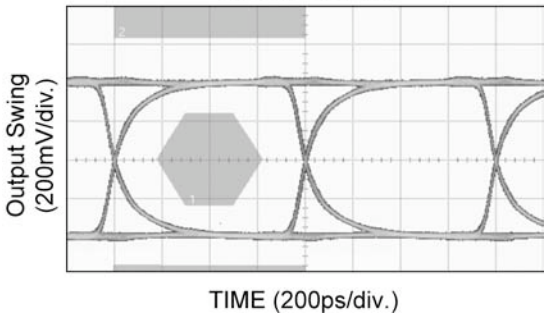
600Mbps Output



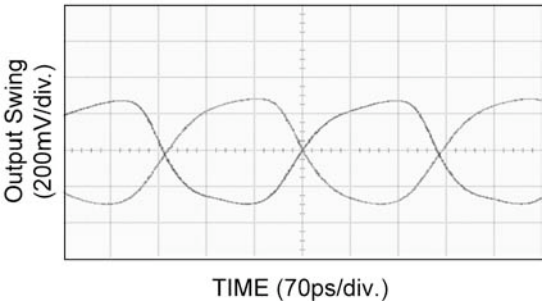
1.25GHz Output



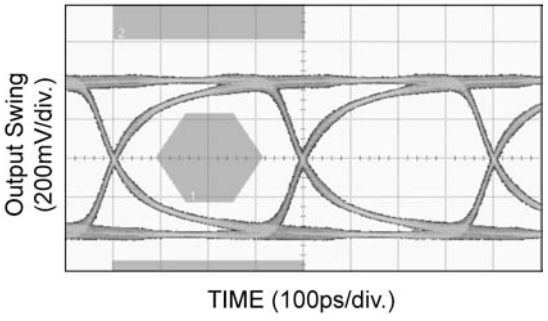
1.25Gbps Output



2.5GHz Output



2.5Gbps Output



Single-Ended and Differential Swings

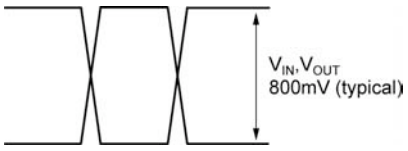


Figure 1a. Single-Ended Voltage Swing

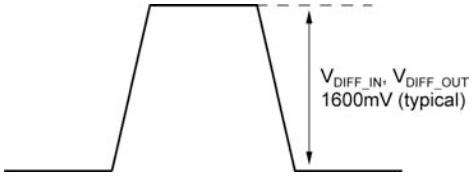
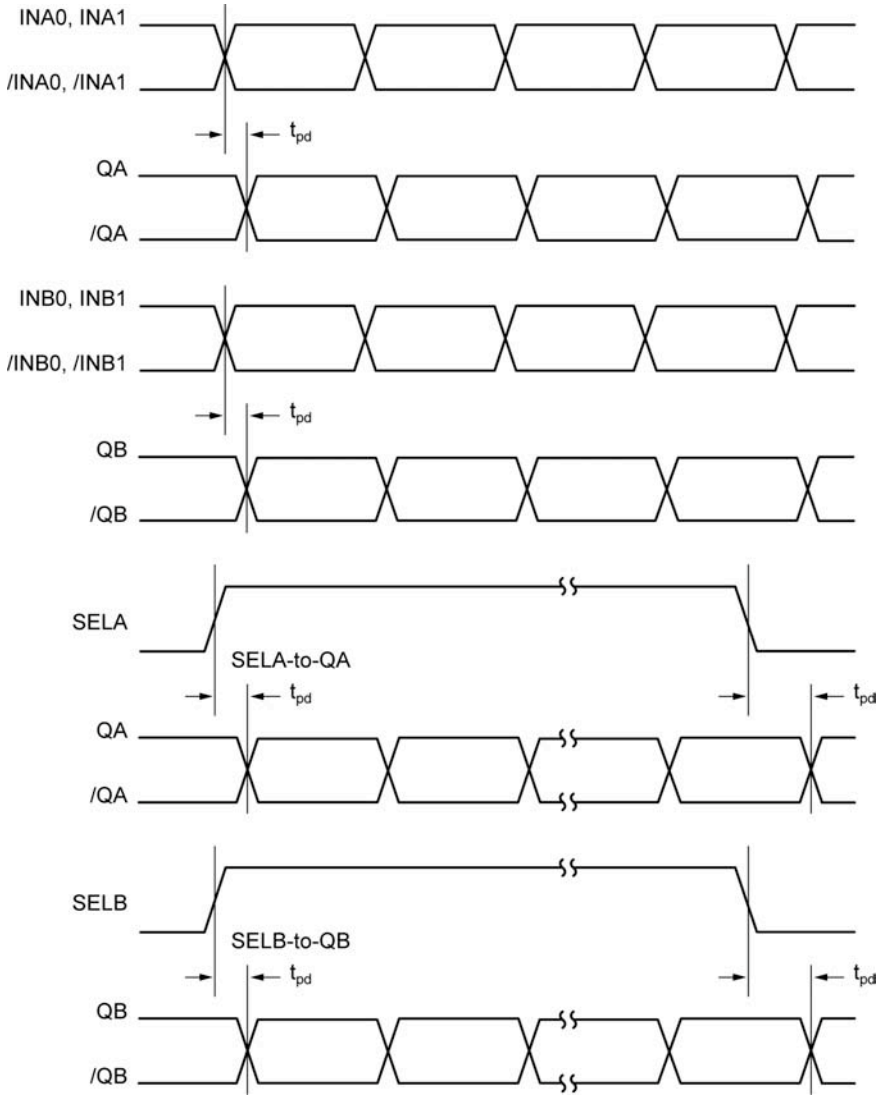


Figure 1b. Differential Voltage Swing

Timing Diagram



Input and Output Stages

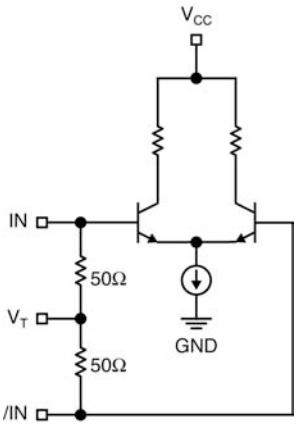


Figure 2a. Simplified Differential Input Stage

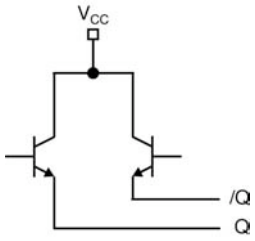


Figure 2b. Simplified LVPECL Output Stage

Input Interface Applications

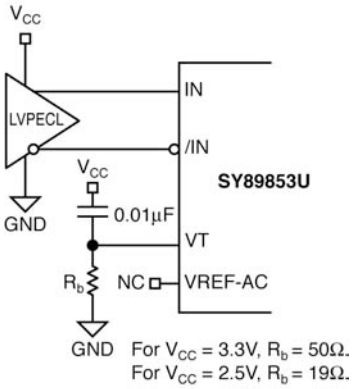


Figure 3a. LVPECL Interface (DC-Coupled)

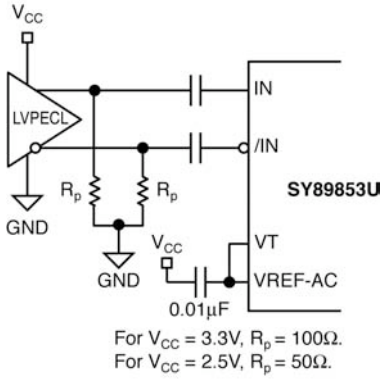


Figure 3b. LVPECL Interface (AC-Coupled)

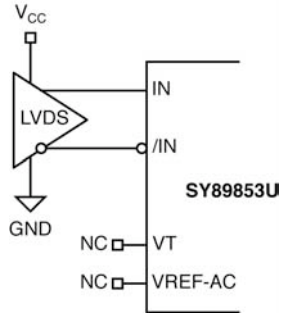
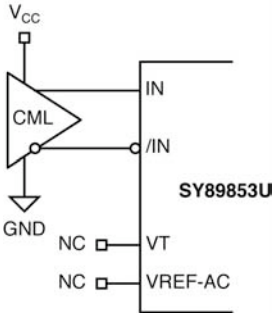


Figure 3c. LVDS Interface



option: may connect V_T to V_{CC}.

Figure 3d. CML Interface (DC-Coupled)

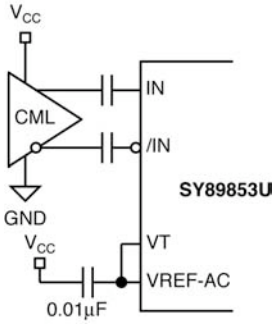
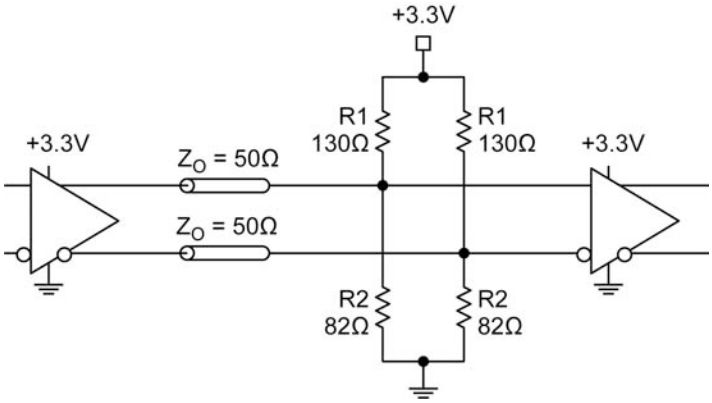


Figure 3e. CML Interface (AC-Coupled)

Output Interface Applications

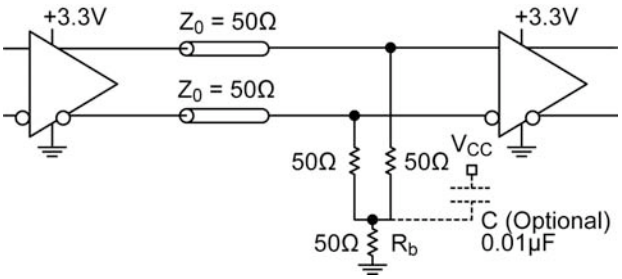
LVPECL has high input impedance, very low output (open emitter) impedance, and small signal swing, which result in low EMI. LVPECL is ideal for driving 50_ and 100_ controlled impedance transmission lines. There are different techniques for terminating LVPECL outputs: Parallel Termination Thevenin-Equivalent, Parallel Termination (3-resistor), and AC-coupled termination. Unused output pairs may be left floating; however, single-ended outputs must be terminated or balanced.



Note:

1. For a 2.5V system, R1 = 250_, R2 = 62.5 _.
2. For a 3.3V system, R1 = 130_, R2 = 82_.

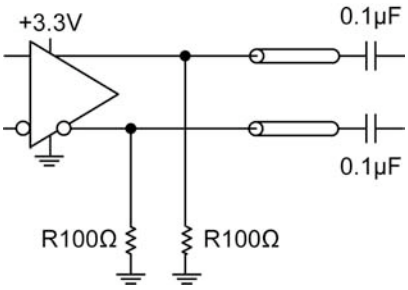
Figure 4a. Parallel Thevenin-Equivalent Termination



Note:

1. For a 2.5V system, R_b = 19_.
2. For a 3.3V system, R_b = 50_.

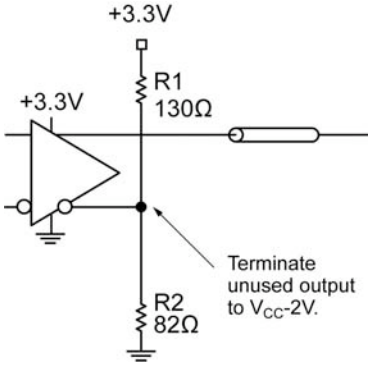
Figure 4b. Parallel Termination (3-Resistor)



Note:

For a 2.5V system, R = 50_.

Figure 4c. AC-Coupled Termination



Note:

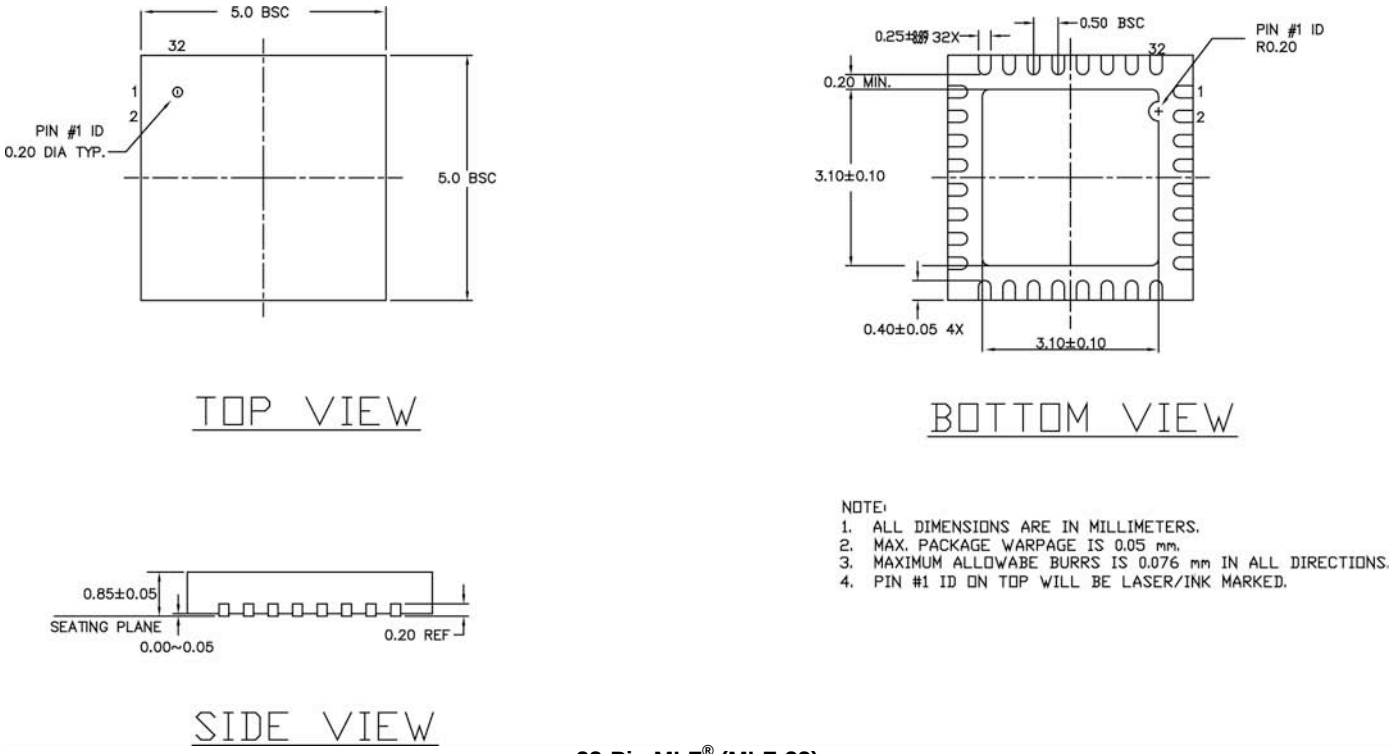
For a 2.5V system, R1 = 250_, R2 = 62.5 _.

Figure 4d. Parallel Thevenin-Equivalent Termination

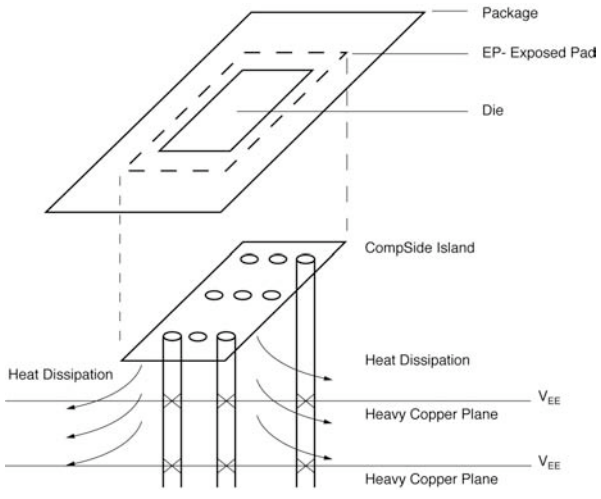
Related Product and Support Documentation

Part Number	Function	Data Sheet Link
SY58026U	5Gbps Dual 2 :1 400mV LVPECL MUX with Internal Termination	www.micrel.com/product-info/products/sy58026u.shtml.
	MLF® Application Note	www.amkor.com/products/notes_papers/MLFAppNote.pdf
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml

Package Information



32-Pin MLF® (MLF-32)



PCB Thermal Consideration for 32-Pin MLF® Package
(Always solder, or equivalent, the exposed pad to the PCB)

Packages Notes:

1. Package meets Level 2 Moisture Sensitivity Classification.
2. All parts are dry-packed before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.

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